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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
CALEY, MICHAEL H

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 04/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/638,403	NAKAYOSHI ET AL.	
	Examiner	Art Unit	
	Michael H. Caley	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *4-8,14,17,18 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,9-13,15,16,19 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08122003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Specie III in the reply filed on 1/18/05 is acknowledged. The traversal is on the ground(s) of Applicant's contention that generic claims are present and that the claims are allowable. This is not found persuasive because no examination on the merits had been conducted at the time of the Restriction/Election Requirement and claims currently stand rejected. Furthermore, the examiner's finding that no claims are generic to all of the identified species may be readily shown in that Specie I does not disclose "a second conductive layer formed on the second insulating layer…in overlapping relation to the drain signal line" as required by claims 1, 11, and 15.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Hanazawa et al. (U.S. Patent No. 5,953,088 "Hanazawa").

Regarding claim 1, Hanazawa discloses a liquid crystal display device having:

a pair of substrates (Figure 5 elements 60 and 84) having a liquid crystal layer (Figure 5 element 90) disposed therebetween;

at least a first conductive layer (Figures 3 and 4 element 53) formed on one of the pair of substrates;

at least a first insulating layer (Figure 4 element 75) formed on the first conductive layer;

a plurality of drain signal lines (Figures 3 and 4 element 50) formed on the first insulating layer in overlapping relation to the first conductive layer;

at least a second insulating layer (Figure 4 elements 79 and 81) formed on the drain signal line;

at least a second conductive layer (Figures 3 and 4 element 51) formed on the second insulating layer and elongated substantially along the drain signal line in overlapping relation to the drain signal line;

wherein the second conductive layer is offset from the overlapping region of the first conductive layer and the drain signal line (Figures 3 and 4).

Regarding claim 2, Hanazawa discloses the second conductive layer as maintaining an electrical connection around the offset region.

Regarding claim 3, Hanazawa discloses a plurality of gate signal lines (Figure 3 element 62) formed on the one of said pair of substrates and crossing the drain signal lines, wherein the

second conductive layer includes a portion having an overlapping relation with the gate signal line (Figures 3 and 5).

Regarding claims 11-13, Hanazawa discloses, in plural pixels, the width of the second conductive layer at the overlapping region of the drain signal line and the first conductive layer (Figure 3 left edge of 51(PE) over 50a) as smaller than a non-overlapping region of the drain signal line and the first conductive layer (Figure 3 center of 51(PE)).

Claims 1-3, 9-13, 15, 16, 19 and 21 rejected under 35 U.S.C. 102(b) as being anticipated by Ohta et al. (U.S. Patent No. 6,208,399 "Ohta").

Regarding claim 1, Ohta discloses a liquid crystal display device having:

a pair of substrates (Figure 2 elements SUB1 and SUB2) having a liquid crystal layer (Figure 2 element LC) disposed therebetween;

at least a first conductive layer (Figures 1 and 4 element CL-g3) formed on one of the pair of substrates;

at least a first insulating layer (Figure 4 element GI) formed on the first conductive layer;

a plurality of drain signal lines (Figure 1 DL, Figure 4 element SD1-D3) formed on the first insulating layer in overlapping relation to the first conductive layer;

at least a second insulating layer (Figures 2 and 4 elements PSV1, PSV2) formed on the drain signal line;

at least a second conductive layer (Figures 1 and 2 element CT) formed on the second insulating layer and elongated substantially along the drain signal line in overlapping relation to the drain signal line;

wherein the second conductive layer is offset from the overlapping region of the first conductive layer and the drain signal line (Figures 1 and 4).

Regarding claim 2, Ohta discloses the second conductive layer as maintaining an electrical connection around the offset region (Figure 1).

Regarding claim 3, Ohta discloses a plurality of gate signal lines (Figure 3 element 62) formed on the one of said pair of substrates and crossing the drain signal lines, wherein the second conductive layer includes a portion having an overlapping relation with the gate signal line (Figures 1).

Regarding claim 9, Ohta discloses a plurality of counter signal lines formed on the one of the pair of substrates and crossing to the drain signal lines, wherein the first conductive layer is a counter signal line (Figure 1).

Regarding claim 10, Ohta discloses the counter signal line as separated into plural lines at the region of overlapping of the drain signal line (Figure 1).

Regarding claims 11-13, Ohta discloses, in plural pixels, the width of the second conductive layer at the overlapping region of the drain signal line and the first conductive layer (Figure 1 along line 8-8) as smaller than a non-overlapping region of the drain signal line and the first conductive layer (Figure 1 along line 6-6).

Regarding claims 15, 16, 19, and 21, Ohta discloses the second conductive layer as having a hole at the overlapping region of the first conductive layer and the drain signal line (Figure 1).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael H. Caley whose telephone number is (571) 272-2286. The examiner can normally be reached on M-F 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael H. Caley
April 2, 2005
mhc

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